AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A method for reducing latency in information transfers to a bus, comprising:

receiving an indication that information is to be transferred from a device to a bus in a first clock cycle and reading a bus grant indication in the first clock cycle;

writing the information to a buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed; and

bypassing the buffer and transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed.

2. (Original) The method according to claim 1, wherein the information includes a write command, an address, and data to be written to the address.

3. (Original) The method according to claim 2, wherein the indication that information is to be transferred to the bus includes the write command.

4. (Original) The method according to claim 1, wherein the information includes a read command and an address from which data is to be read.

5. (Original) The method according to claim 4, wherein the indication that information is to be transferred to the bus includes the read command.

6. (Original) The method according to claim 1, wherein access to the bus is controlled by a bus arbiter employing a bus parking protocol.

7. (Original) The method according to claim 6, further comprising sending a bus access request to the bus arbiter if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

8. (Original) The method according to claim 7, further comprising periodically sending bus access requests to the bus arbiter and reading the bus grant indication if the information stored in the buffer has not been transferred to the bus, so that when the bus grant indication indicates that

transfer of the information to the bus is allowed, the information stored in the buffer is transferred to the bus.

9. (Currently Amended) A bus interface unit for reducing latency in information transfers from a device to a bus, comprising:

a buffer having inputs coupled to the device; and

logic configured to receive an indication from the device in a first clock cycle that information is to be transferred to the bus, read a bus grant indication in the first clock cycle, and cause the information to either be stored in the buffer if the bus grant information does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed.

10. (Original) The bus interface unit according to claim 9, wherein the information includes a write command, an address, and data to be written to the address.

11. (Original) The bus interface unit according to claim 10, wherein the indication from the device that information is to be transferred to the bus includes the write command.

12. (Original) The bus interface unit according to claim 9, wherein the information includes a read command and an address from which data is to be read.

13. (Original) The bus interface unit according to claim 12, wherein the indication from the device that information is to be transferred to the bus includes the read command.

14. (Original) The bus interface unit according to claim 9, wherein access to the bus is controlled by a bus arbiter employing a bus parking protocol.

15. (Original) The bus interface unit according to claim 14, wherein the logic is further configured to send a bus access request to the bus arbiter if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

16. (Original) The bus interface unit according to claim 15 wherein the logic is further configured to periodically send bus access requests to the bus arbiter and read the bus grant indication if the information stored in the buffer has not been transferred to the bus, so that when the bus grant indication indicates that transfer of the information to the bus is allowed, the logic causes the information stored in the buffer to be transferred to the bus.

17. (Original) The bus interface unit according to claim 9, wherein the logic includes a multiplexer having first inputs coupled to the buffer inputs, second inputs coupled to the buffer outputs, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and the logic is further configured to provide a control output to the at least one select input so that the first inputs are coupled to the outputs if the bus grant indication indicates that transfer of the information to the bus is allowed and the buffer is empty.

18. (Original) The bus interface unit according to claim 17, wherein the logic is further configured to provide the control output to the at least one select input so that the second inputs are coupled to the outputs if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

19. (Currently Amended) In a computer system including a bus with access governed by a bus arbiter employing a bus parking scheme and a buffer having inputs coupled to a device so that information to be transferred from the device to the bus is stored in the buffer if a bus grant indication generated by the bus arbiter indicates that the bus is unavailable for the transfer, a buffer bypass circuit for reducing latency in information transfers to the bus comprising:

a multiplexer having first inputs coupled to inputs to the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and

logic configured to receive an indication from the device in a first clock cycle that information is to be transferred to the bus, read a bus grant indication in the first clock cycle, and provide control information to the at least one select input such that the first inputs are coupled to the

outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus.

20. (Previously Presented) The buffer bypass circuit claimed in claim 19, wherein the logic is further configured to provide control information to the at least one select input generated such that after checking the bus grant indication the second inputs are coupled to the outputs of the multiplexer if the buffer is not empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus, or the bus grant indication does not indicate that the bus is available for transfer of the information to the bus.

21. (Original) The buffer bypass circuit according to claim 19, wherein the information includes a write command, an address, and data to be written to the address.

22. (Original) The buffer bypass circuit according to claim 19, wherein the information includes a read command and an address from which data is to be read.

23. (Previously Presented) The buffer bypass circuit according to claim 19, wherein the logic is further configured to send a bus access request to the bus arbiter if the bus grant indication does not indicate that the bus is available for transfer of the information to the bus.

24. (Currently Amended) The buffer bypass circuit according to claim 23, wherein the logic is further configured to periodically send bus access requests to the bus arbiter and read the ensuing bus ~~grants~~ grant indications generated by the arbiter in response to the bus access requests if the information stored in the buffer has not been transferred to the bus, so that when one of the bus grants ~~grants~~ grant indications indicates that the bus is available for transfer of the information to the bus, the information stored in the buffer is transferred to the bus.